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Recoverable Data Acquisition System Designed and Developed for Penetrator Applications

T. F. F. Eklund, D. C. Stoner

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RECOVERABLE DATA ACQUISITION SYSTEM DESIGNED AND DEVELOPED FOR PENETRATOR APPLICATIONS

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ABSTRACT

The requirement for a recoverable data acquisition system capable of storing high frequency, high-g impact strain and acceleration data on penetrator vehicles resulted in the development of a small versatile recording package.

DOD
MCL
b(3)

Acknowledgments

The authors wish to thank D. Hardin for his expertise in computer programming for data playback operations, R. Roberson for his original investigation and checkout of the signal conditioning, and C. Frost for his extensive potting procedures investigation.

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LIVERMORE DATA RECOVERY SYSTEM

Introduction

The Livermore Data Recovery System is a high speed recoverable data acquisition system. It stores digitized data in 80,000 bytes on-board, static Random Access Memory (RAM) and has a full eight bit flash analog to digital converter (ADC) to service up to 32 channels of strain and acceleration data with an additional 16 channels of bi-level inputs. See Tables IV through VII in Appendix A for typical data list requirements. All control circuitry, signal conditioning, power supply module, and memory are contained in one seven inch diameter, four and one half inch long cylinder that weighs less than 10 pounds. This is larger in diameter and relatively shorter than previous Sandia National Laboratories, Albuquerque (SNLA) penetrator memory systems. The larger diameter instrumentation was used primarily because it was easier to house the electronics for the SNLL penetrator projects. Because of the very high axial accelerations, it was expected that the larger diameter electronics package might experience difficulties. In fact, no such difficulties occurred.

The SEP version of the LDRS stores 0.2 seconds of single format data in the RAM at a rate of 400,000 samples per second (sps). Modified for the ASP version, multiple formats and data record rates are pre-programmed to optimize memory usage and increase record time. The ability to store decommutator synchronization in the memory or insert synchronization post test is also available, along with the option of basing the format on 256 or 192 words per frame to best utilize the desired number of channels and frequency response on any given vehicle.

Once the vehicle is recovered, the LDRS is removed and the data is off loaded in either parallel form into a computer or serial form into a decommutator. Reading the data out does not destroy the contents of memory and the back up battery system is designed to retain the data for up to six months.

Functional Description

Overview

The LDRS system power is an on-board +18 volt rechargeable nickel cadmium (NiCad) battery. The major portion of the control circuitry is implemented with the CD4000 series CMOS integrated circuit (IC) logic powered by +5 volts dc. Each system control command is initiated with +28 volts dc and a mode monitor is provided to verify system mode of operation; i.e. reset, armed (continuously writing into memory), triggered, or reading (playback). System clocks are based on free running, astable multivibrators with the frequency dependant on the RC time constant selected. Record and playback rates are independent of each other and use separate circuits to generate the desired frequencies. Reference System Block Diagram next page.

The various inputs are selected according to a pre-determined format via a look-up table programmed in the fuse link Programmable Read Only Memory (PROM). The PROM provides the address and enable signals to the two 16 channel CMOS analog multiplexers and the two eight bit digital latching buffers. The multiplexed analog signal is converted to an eight bit digital representation and stored in the next available memory location. Once the maximum memory address (81920) has been reached, the address generator resets to zero. That is, a new set of data is constantly being written into memory until a trigger signal is received. The trigger signal allows a counter to time out which subsequently halts the writing process, thus saving the pre-determined amount of pre- and post-trigger data.

If the stored data is actually shot data (versus laboratory test data), the memory contents is retained by a back-up battery until the vehicle is recovered and the LDRS package removed. In either case, a read command may now be initiated to output the data in either serial or parallel format. The serial pulse train (5460 bits per second) is Non-Return to Zero Level (NRZL) format and must have synchronization (sync) words either stored in RAM during the write cycle or inserted post test. This pulse train is fed into a decommutator which locks on the sync words and separates out and displays the individual channels. The parallel data is read out of memory one byte (eight bits) at a time at 682.5 bytes per second. This playback format requires no synchronization and is transferred directly into a computer which performs the decommutation process and represents each channel graphically in engineering units versus time. See Appendix A, Table I for complete system specifications.

The following sections provide more in-depth descriptions of the various circuit functions and timing relationships as well as testing and assembly procedures.

TABLE I
NORMAL SEQUENCE OF EVENTS

Lab Test

-Power on
-Reset*
-Arm*
-Trigger*
-Read on
-Read off
-Power off

Flight Test

T-10 min	-External power on
"	-Reset
"	-Arm
T-8 min	-Trigger
"	-Read on
T-6 min	-Read off
"	-Reset
"	-Arm
T-5 min	-Internal power on (i.e. squib fire)
"	-External power off
"	-Trigger
T-4 min	-Read on
T-2 min	-Read off
"	-Reset
"	-Arm
"	-Trigger
T-90 sec	-Read on
T-60 sec	-Read off
"	-Reset
"	-Arm
T0	-Penetrator fire
	-Recovery
	-Disassembly
	-External power on
	-Read on
	-Read off
	-External power off
	-Plot data

* momentary switch function

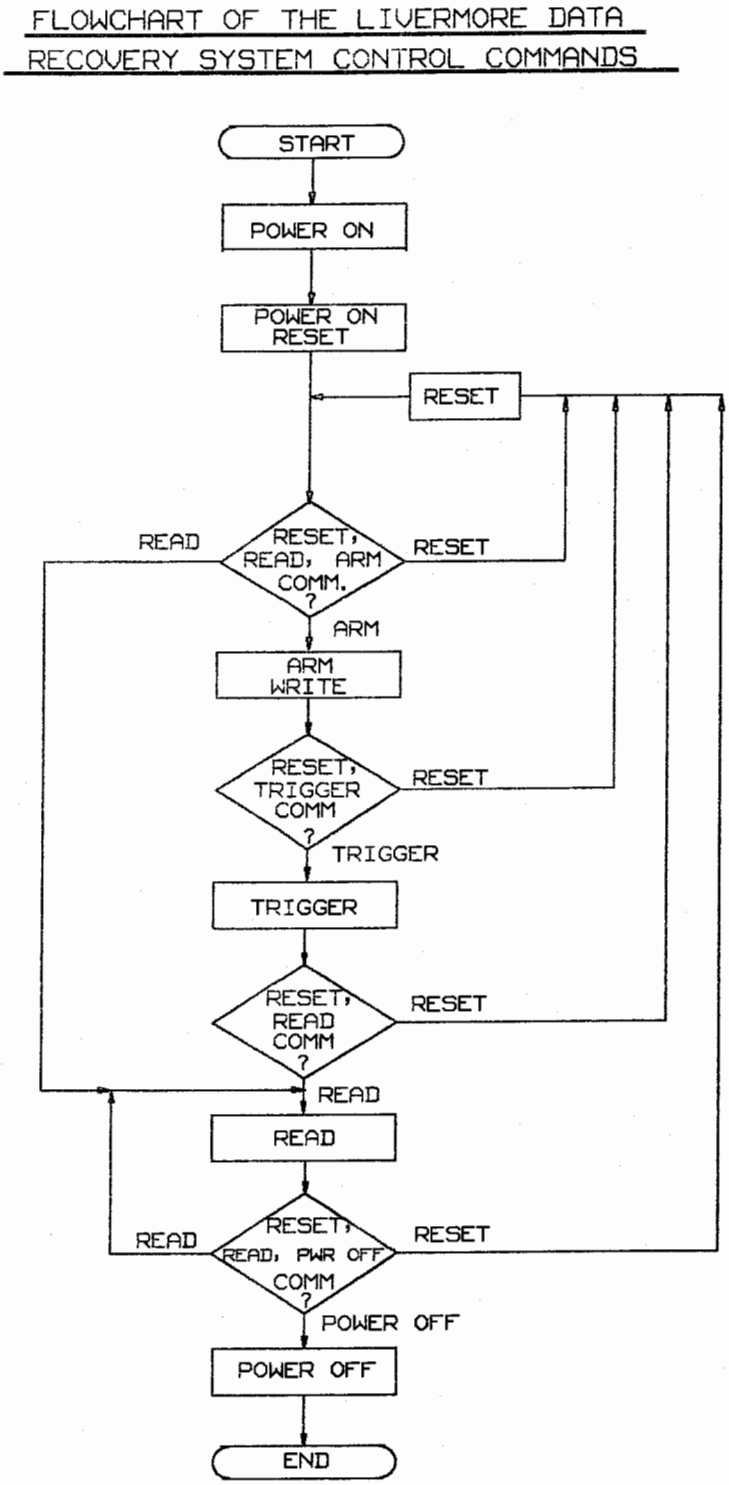


FIGURE 7. System Control Command Flowchart

Control and Memory

As previously mentioned in the overview, all system control functions (reset,arm,trigger,read) are initiated by applying +28 volts dc to the correct J2 interface pin (see System Schematic, Appendix B-1). The control signals are passed through the "mother board" to the "control board" where they are lowered to +5 volts via a simple resistor network voltage divider. The purpose in using +28 volts for the control functions is so that no other voltage available to the LDRS (i.e. internal or external power) is high enough to initiate a control function.

The "Reset" function, which may be initiated any time (Refer to Fig. 7), provides output disables to the various latches and reset or clear signals to the flip flops, counters, and multivibrators. The reset command must be removed prior to activating any other commands.

When the "Arm" command is initiated, preceded by a "Reset", many circuits are enabled or preset to a specific state. The first circuit enabled is the record rate clock, CD4047 astable multivibrator, which is set up to run the system at a sample rate of 400 K sps for SEP and 160 K sps for ASP. Also enabled is the memory address generator, which consists of a 12 stage high speed ripple-carry binary counter (74HC4040) with a CD4013 "D" type flip flop used as the 13th stage to produce a count of 8191, plus a decade counter (CD4017) used to sequentially select one of the ten memory IC's.

As the binary counter changes from the maximum count of 8191 back to zero, the decade counter (memory chip select) increments one count. When the decade counter reaches it's maximum count, which selects RAM chip #10, it too resets to zero, thus selecting RAM chip #1. This recycling of the memory address generator provides for continuous updating of new data in the RAM. The only exception to selecting all ten memory chips would be if the format was based on 192 words per frame instead of 256. In which case the decade counter would only count up to eight, thus not selecting the last RAM chip. This reduces the total memory size to 73728 bytes, but is necessary to maintain compatibility between the format stored in the PROM and the memory address generator.

The Harris HM6616 2K x 8 CMOS PROM located on the input board provides the method for selecting specific inputs in the proper sequence (see Appendix A Tables IV,V,VI). The PROM address generator, consisting of two four bit synchronous counters, runs at the same rate as the RAM address generator in both record and playback modes. In the record mode, the PROM provides the analog multiplexer chip enable and the four bits of multiplexer address. The PROM also enables the Harris 82C82 CMOS octal latches used for bi-level inputs and sync word enable. When bit 7 (msb) of the PROM is high, each of the eight PROM outputs become the corresponding bit in the sync word itself. The following table is a bit by bit description of the PROM.

TABLE II
LOOK-UP TABLE PROM BIT DESIGNATION

Bit 7.....0 = data word
1 = sync word
Bit 6.....0 = digital word one (DW1) selected and stored in RAM
1 = digital word two (DW2) selected and stored in RAM
Bit 5.....0 = analog word stored in RAM
1 = digital word stored in RAM
Bit 4.....0 = analog mux #1 selected for input
1 = analog mux #2 selected for input
Bits 3,2,1,0.....designates which input (0 thru 15) is selected on a given analog mux to be stored in RAM during the next word time

The timing relationships between PROM output, digital word input, analog word input, and analog to digital conversion are very critical (see Timing Diagram on next page). To allow for maximum settling time of an analog input through the multiplexer, the analog inputs are enabled by the PROM almost an entire word time (2.5 uSec for 400 Ksps) prior to the convert pulse. To accommodate the conversion at the end of a word time, the digitized data is stored in RAM during the following sample. However, a sync word or set of eight bi-level inputs is both sampled and stored in RAM during the same word time.
Table III is a short example illustrating this method of sampling and storing the data.

TABLE III
SAMPLING/STORING DATA

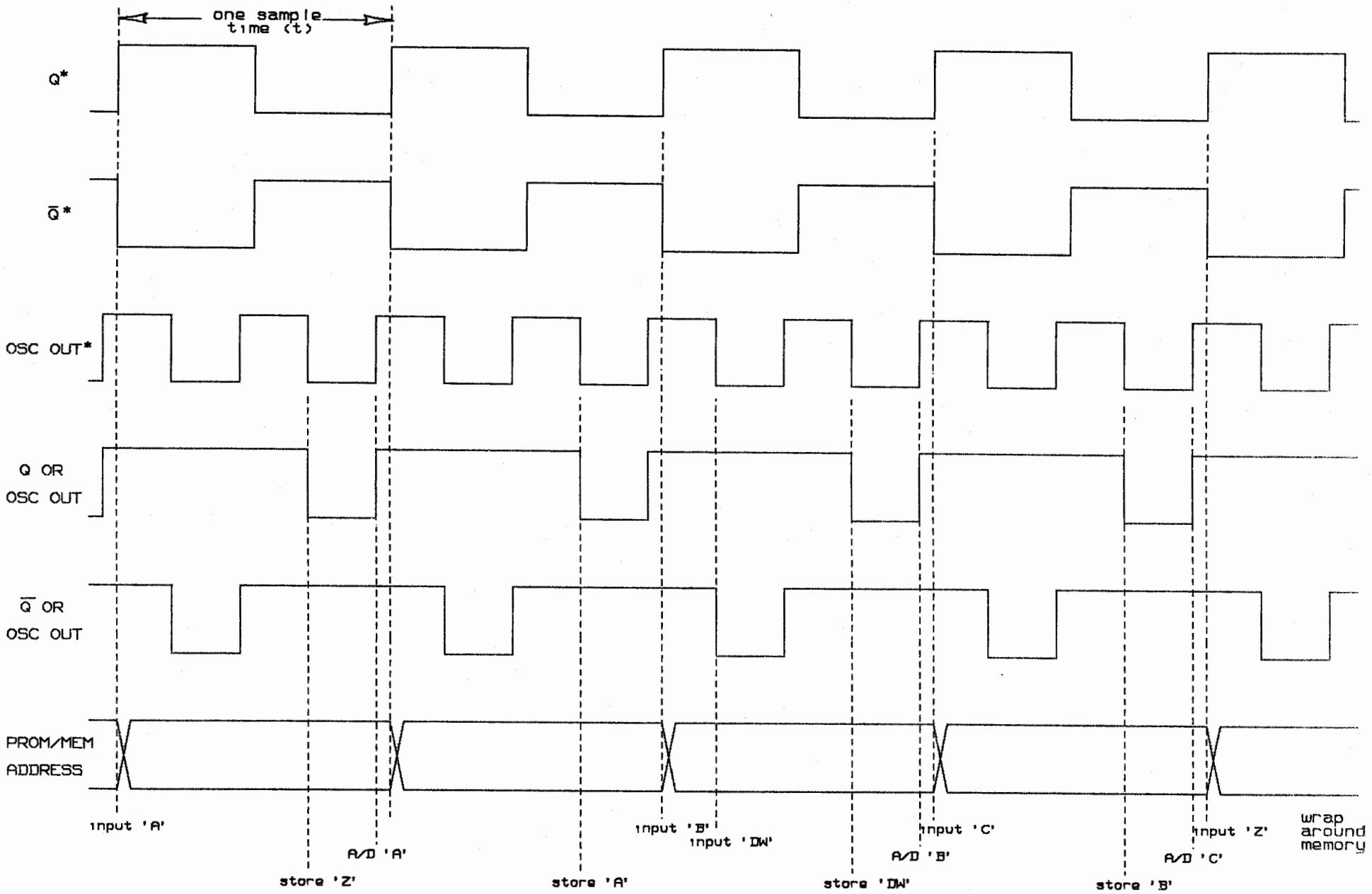
format output	mux input
A1-1	A1-2
A1-2	none
DW1	DW1/A2-1*
A2-1	A2-2
A2-2	A1-1

* note: Both DW1 and A2-1 are sampled at the same time, however, DW1 is stored in RAM during this word time and A2-1 is stored in RAM during the next word time.

There are two methods of initiating a "Trigger" command. One method is by momentarily applying +28 volts dc to the J2 connector pin labelled "TRIG". The other is to provide sufficient acceleration in the proper direction to overcome the bias level preset on the comparator input labelled "TRIG (INT)" on the control board.

The output of the comparator is provided with a jumper option which is set depending on accelerometer orientation and whether a trigger is desired on gun barrel exit (Davis gun shot) or impact (rocket shot).

In either case, a "Trigger" signal allows the CD40103 pre-settable counter to start counting every other frame of data. When the counter reaches it's terminal count of zero, it provides a carry out signal which stops the system from writing into memory. The counter pre-set value determines the number of



t = 2.5 uSec for SEP (400 KHz)
t = variable for ASP
* = CD4047 output (record rate gen)

FIGURE 8. Data Record Mode Timing Diagram

pre-trigger frames that are retained in memory. The formula for calculating frames of pre-trigger is as follows:

Eq. (1) $F_p = F_t - 2C - 2$ where: F_p = frames of pre-trigger
F_t = total frames (320 or 384)
C = counter pre-set value

Normally the user chooses the amount of pre-trigger desired, then solves for the counter pre-set value using the following equation:

Eq. (1.1) $C = (F_t/2) - (F_p/2) - 1$

The counter pre-set value is then converted to a binary value and the proper jumpers installed on the "control board".

To retrieve the data stored in RAM, the system is connected as in Fig. 9 and a "Read" command is continuously applied. Each time the "Read" command is initiated, RAM address zero is output first regardless of where the last write or read was terminated. The two methods of playback available to the operator are serial and parallel. Serial mode is chosen when the user desires to look at the data on a decommutator and is initiated by applying both "Read" and "Serial" commands. Putting the system in serial playback mode outputs 5460 bits per second of NRZL data with three words of synchronization at the beginning of each frame. These sync words replace samples of gage data and are superimposed in the pulse train without changing the actual value of the sample stored in RAM. However, the option to store sync in memory during the record mode is available. The sync words selected are FA,F3,A0 (hex), but may be programmed to other patterns.

Parallel data mode is used to down load the contents of memory to a computer. Parallel data is output at 682.5 bytes per second and does not require sync words because with the RAM address zero being selected first, the computer can keep track of all channel positioning. The computer performs all decommutating operations and produces plots of each data channel with engineering units conversion already applied.

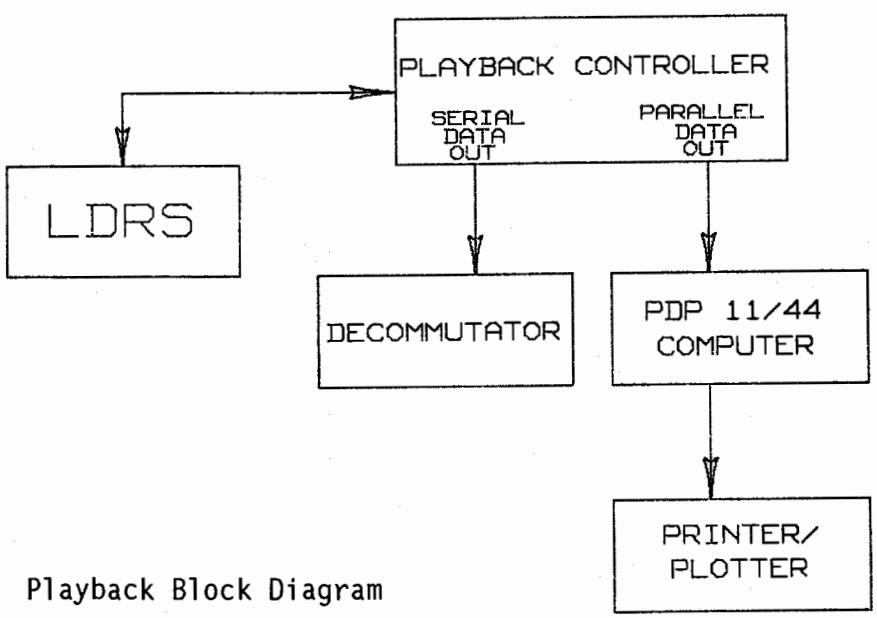


Figure 9. Playback Block Diagram

The "mode monitor" circuit, located on the "control board", (Appendix B Fig. 8) was implemented as a means of verifying proper operation of the system. It consists of three digital signals feeding an analog summing amplifier set up as a voltage follower. In the "Reset" position, all three signals ($\overline{WR}$,$\overline{RD}$,$\overline{Q}_{trig}$) are high. As the three signals are inverted, this produces 0.0 volts on the amplifier input. In the "Arm" position, the $\overline{WR}$ signal goes low and 1.0 volts appears on the mode monitor. When a trigger signal is initiated, resulting in a memory write stop pulse, the $\overline{WR}$ goes back high and the $\overline{Q}_{trig}$ signal goes low. This produces 2.4 volts on the mode monitor. This signal stays low until a "Reset" command is initiated. When the "Read" command is applied (serial or parallel), the $\overline{RD}$ line goes low and the combination of the two signals produces 3.6 volts on the amplifier. See Table IV for list of control functions and corresponding mode monitor levels.

TABLE IV
QUICK REFERENCE GUIDE TO LDRS CONTROL FUNCTIONS

Function	Mode Mon	Description
RESET	0.0 volts	-Not "writing" (record) -Not "reading" (playback) -Must be done prior to "ARM" -Can be done any time -Can go to "READ" mode directly -Cannot "TRIGGER" from here
ARM	1.0 volts	-"writing" -not "reading" -can only follow a "RESET" -cannot go to "READ" directly -must precede "TRIGGER" -can "RESET" -continuously updating memory
TRIGGER	2.4 volts	-initiates memory stop counter -must "ARM" prior to "TRIGGER" -can "READ" after mem stop cntr -can "RESET" -cannot go to "ARM" directly
READ	3.6 volts	-"reading" memory continuously -not "writing" -cannot "READ" if in "ARM" mode -can "RESET" -can turn "READ" off and on again -starts "reading" at address zero

The filtering network in each signal conditioning circuit consists of two stages of a two-pole Bessel filter. The 6db point (quarter power) is determined by the sample rate (samples per second divided by five) and set by selecting the proper resistor value (see table on "Accelerometer Signal Conditioning" in Appendix B-4).

The two 8 bit digital word inputs are physically located on the input board and consist of a non-inverting buffer amplifier set up with a gain of one feeding a latch input. The amplifier input is shunted to ground with a 30.1 K ohm resistor, so when the input is floating, a logic zero results. These channels were designed to monitor switches that are normally pulled high, such as crack detectors that monitor the integrity of various mechanical parts. When the switch opens, the 30.1 K ohm resistor pulls the input low, producing a change on the input. Another use of this circuit is to monitor a digital signal (0 or +5 volts). For example, the interface drawing in Appendix B Fig. 2 shows the T0 trigger signal and seven bits of the memory address generator being monitored by one of these digital word inputs. This was done for diagnostic purposes.

The last two types of signals that can be monitored are the system power and pressure gages. This requires modifying the existing circuitry on either the accelerometer or strain gage circuits. To monitor a simple dc voltage, the gain is replaced with a voltage divider to bring the monitored voltage into the 0 to +5.1 volt range. To monitor the pressure gages on the water entry (ASP) shots, external signal conditioning is used, and the amplifier is modified for a gain of one.

Potting and Assembly Procedures

After a system has been totally checked and verified to be working properly, each printed wiring board (PWB) is encased in a foam type potting material. The potting material is the CPR 1024 Potting Foam System. The density of the material is varied by the packing or the amount of foam allowed to cure in a given volume. The mother board is potted with 30 pound foam (30 lb per cubic foot), the battery board is potted with 50 pound foam and the balance of the boards in 20 pound foam. To ensure the correct density, an aluminum potting mold of known volume is fitted around the PWB and the thick liquid material is evenly poured on both sides of the board. The whole assembly is then cured at 150°F for 16 to 18 hours. The foam is then machined to the specifications listed on the "Potted Module" drawings in Appendix C Figs. 6 and 7.

When the system is stacked and ready to install in the "LDRS Case" (see next two photos), rubber shims are placed in the bottom of the case. Then a pre-load pressure of 10,000 pounds is applied to the lid using a calibrated press and the lid bolts are tightened. The stack is then potted into the case using heat cured expanding foam beads. The beads are fed into the case via holes in the side of the case, and the assembly is placed in a 250°F, pre-heated oven for 15 minutes, then immediately cooled in a 32°F oven for five minutes and 70°F for 15 minutes.

Environmental Testing

DOD
NCTL
b(3)

Field Testing

DOD
NCTL
b(3)

Problems and Future Development

DOD
NCTL
b(3)

The NiCad primary battery has either failed completely or experienced a transient reduction in voltage on almost every field test. See photo of damaged flight test battery (Fig. 12), noting displacement of cells. The first attempted solution was to add a fifth cell, raising the voltage from 14.4 to 18.0 volts. This seemed to help the transient voltage drop some, but provided no assistance when a total failure occurred. The second attempted solution was to add an identical battery pack external to the LDRS, mounted upside down inside the penetrator vehicle. With only a sample of one test, it has not been determined if this increased the chance of acquiring good data. The best solution would be to develop a battery that can withstand a higher g loading than is presently available.

The second problem that needs addressing is the lateral movement of the stacked printed wiring boards inside the LDRS case. Only a partial curing (expansion and adhesion) of the beads was ever accomplished. To totally cure the beads, a higher and/or longer temperature is required. By empirical data it is feared the higher temperature would damage the internal electronic parts. A new material and method of curing is being investigated.

The main problem experienced in all three ASP tests was the moisture that entered the LDRS case. Two were totally immersed in water and the third unit had what looked like condensation inside the case. An attempt will be made to seal the LDRS case for subsequent water shots.

Conclusion

The Livermore Data Recovery System has fulfilled the requirement for a recoverable data acquisition system. It has proven its ability to record high frequency, high-g impact environmental data in the laboratory and in the field for both the earth and water penetrator applications. The performance and survivability of the LDRS are expected to improve as the on-board battery system becomes more reliable.

APPENDIX A

SPECIFICATIONS

Table A-I System Specifications

Table A-II Board Descriptions

Table A-III Typical Channel Assignments

Table A-IV Typical Generic Format

Table A-V Typical Format

Table A-VI Typical Format Query

TABLE A-I
LIVERMORE DATA RECOVERY SYSTEM

SPECIFICATIONS

Electrical

DOD
NRTL
b(3)

TABLE A-III. Typical Channel Assignments

TEST SERIES: DSP-200

TEST VEHICLE: DSP-204

LDRS SYSTEM: 108

DATE: 8/17/87

TABLE A-IV. Typical Generic Format

DSP204G

256 WORDS/FRAME
640 microSEC/FRAME
2.5 microSEC/WORD (400000 W/SEC)

	0	1	2	3	4	5	6	7
1	B1	B2	B3	B4	B5	C1	C2	C3
2	B6	B7	B8	B9	B10	C4	C5	D1
3	B1	B2	B3	B4	B5	C6	C7	D2
4	B6	B7	B8	B9	B10	C8	C9	DW1
5	B1	B2	B3	B4	B5	C1	C2	C3
6	B6	B7	B8	B9	B10	C4	C5	D3
7	B1	B2	B3	B4	B5	C6	C7	D4
8	B6	B7	B8	B9	B10	C8	C9	DW1
9	B1	B2	B3	B4	B5	C1	C2	C3
10	B6	B7	B8	B9	B10	C4	C5	D1
11	B1	B2	B3	B4	B5	C6	C7	D2
12	B6	B7	B8	B9	B10	C8	C9	DW1
13	B1	B2	B3	B4	B5	C1	C2	C3
14	B6	B7	B8	B9	B10	C4	C5	D3
15	B1	B2	B3	B4	B5	C6	C7	D4
16	B6	B7	B8	B9	B10	C8	C9	DW1
17	B1	B2	B3	B4	B5	C1	C2	C3
18	B6	B7	B8	B9	B10	C4	C5	D1
19	B1	B2	B3	B4	B5	C6	C7	D2
20	B6	B7	B8	B9	B10	C8	C9	DW1
21	B1	B2	B3	B4	B5	C1	C2	C3
22	B6	B7	B8	B9	B10	C4	C5	D3
23	B1	B2	B3	B4	B5	C6	C7	D4
24	B6	B7	B8	B9	B10	C8	C9	DW1
25	B1	B2	B3	B4	B5	C1	C2	C3
26	B6	B7	B8	B9	B10	C4	C5	D1
27	B1	B2	B3	B4	B5	C6	C7	D2
28	B6	B7	B8	B9	B10	C8	C9	DW1
29	B1	B2	B3	B4	B5	C1	C2	C3
30	B6	B7	B8	B9	B10	C4	C5	D3
31	B1	B2	B3	B4	B5	C6	C7	D4
32	B6	B7	B8	B9	B10	C8	C9	DW1

CH	SPS	HZ	# of CH
B	25000	5000	10
C	12500	2500	9
DW	12500	2500	1
D	6250	1250	4

TABLE A-V. Typical Format

DSP204

256 WORDS/FRAME
640 microSEC/FRAME
2.5 microSEC/WORD (400000 W/SEC)

	0	1	2	3	4	5	6	7
1	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
2	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT1
3	AX-1	AX-2	AY-1	S1	S2	S9	S10	BATT2
4	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
5	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
6	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT3
7	AX-1	AX-2	AY-1	S1	S2	S9	S10	CAP
8	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
9	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
10	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT1
11	AX-1	AX-2	AY-1	S1	S2	S9	S10	BATT2
12	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
13	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
14	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT3
15	AX-1	AX-2	AY-1	S1	S2	S9	S10	CAP
16	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
17	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
18	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT1
19	AX-1	AX-2	AY-1	S1	S2	S9	S10	BATT2
20	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
21	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
22	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT3
23	AX-1	AX-2	AY-1	S1	S2	S9	S10	CAP
24	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
25	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
26	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT1
27	AX-1	AX-2	AY-1	S1	S2	S9	S10	BATT2
28	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0
29	AX-1	AX-2	AY-1	S1	S2	S3	S4	BUSS
30	AY-2	AZ-1	AZ-2	S5	S7	S6	S8	BATT3
31	AX-1	AX-2	AY-1	S1	S2	S9	S10	CAP
32	AY-2	AZ-1	AZ-2	S5	S7	S11	S12	T0

	SPS	HZ	# of CH
ACCEL	25000	5000	6
STRAIN	25000	5000	4
STRAIN	12500	2500	8
VOLTMON	12500	2500	1
DW	12500	2500	1
VOLTMON	6250	1250	4

BUSS = 18v INT PWR
BATT1= 18v INT BATT
BATT2= 28v EXT BATT
BATT3= 18v EXT BATT
CAP = WES CAP MON
T0 = T0 & MEM ADD

TABLE A-VI. Typical Format Query

DSP204
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FORMAT DATA QUERY TABLE

	GEN	NAME	MUX	H2NEXT	H1NEXT	H1THIS
1	B1	AX-1	A1-01	0	0	0
2	D2	BATT2	A1-02	1	0	0
3	C1	SG-3A	A1-03	2	0	0
4	B9	SG-5A	A1-04	3	0	0
5	B3	AY-1	A1-05	4	0	0
6	B6	AY-2	A1-06	5	0	0
7	C8	SG-11A	A1-07	6	0	0
8	D4	CAP	A1-08	7	0	0
9	D3	BATT3	A1-09	8	0	0
10	C3	BUSS	A1-10	9	0	0
11		NOTUSED	A1-11	A	0	0
12	C4	SG-6H	A1-12	B	0	0
13	B10	SG-7A	A1-13	C	0	0
14	C6	SG-9H	A1-14	D	0	0
15		NOTUSED	A1-15	E	0	0
16	D1	BATT1	A1-16	F	0	0
17	B4	SG-1A	A2-01	0	1	0
18		NOTUSED	A2-02	1	1	0
19	C2	SG-4A	A2-03	2	1	0
20	B2	AX-2	A2-04	3	1	0
21	C5	SG-8H	A2-05	4	1	0
22	C7	SG-10H	A2-06	5	1	0
23	C9	SG-12A	A2-07	6	1	0
24	B8	AZ-2	A2-08	7	1	0
25		NOTUSED	A2-09	8	1	0
26	B5	SG-2A	A2-10	9	1	0
27		NOTUSED	A2-11	A	1	0
28		NOTUSED	A2-12	B	1	0
29		NOTUSED	A2-13	C	1	0
30		NOTUSED	A2-14	D	1	0
31	B7	AZ-1	A2-15	E	1	0
32		NOTUSED	A2-16	F	1	0
33	DW1	TO/MAD	D1	0	0	10
34			D2	0	0	110
35	SW1	SYNC-1	SW1	0	0	1101
36	SW2	SYNC-2	SW2	A	0	1101
37	SW3	SYNC-3	SW3	3	0	1000

APPENDIX B

SCHEMATICS

Figure B-1 System Schematic

Figure B-2 Typical Interface

Figure B-3 Mother Board Schematic

Figure B-4 Accelerometer Signal Conditioning Schematic

Figure B-5 Strain Gage Signal Conditioning Schematic

Figure B-6 Input Board Schematic

Figure B-7 Memory Board Schematic

Figure B-8 SEP Control Board Schematic

Figure B-9 ASP Control Board Schematic

Figure B-10 Internal Power Supply Schematic

DOD
NCP L
b(5)

DOD
NCTL
b3)

DOD
MCTL
b(3)

APPENDIX D

PRINTED WIRING BOARD PHOTOGRAPHS

Figure D-1 Mother Board

Figure D-2 Accelerometer Signal Conditioning Board

Figure D-3 Strain Gage Signal Conditioning Board

Figure D-4 Input Board

Figure D-5 Memory Board

Figure D-6 SEP Control Board

Figure D-7 ASP Control Board

Figure D-8 Power Supply Board

b(3)

DOD
MCL
b(3)

APPENDIX E

TYPICAL DATA PLOTS

Figure E-1 DSP 204 Shot data - Accelerometer (AX-1)

Figure E-2 DSP 204 Shot data - Strain gage (SG-1)

Figure E-3 DSP 204 Shot data - Battery monitor (BATT-1)

Figure E-4 DSP 204 Shot data - Trigger and memory monitor (TO)

Figure E-5 RAP 201 Shot data - Pitch gyro (GYP-1)

Figure E-6 RAP 201 Shot data - Pressure (P-1)

FIGURE E-1. DSP 204 Shot Data - Accelerometer (AX-1)

FIGURE E-3. DSP 204 Shot Data - Battery Monitor (BATT-1)

DOD
b(3)

FIGURE E-5. RAP 201 Shot Data - Pitch Gyro (GYP-1)

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